**Design and Analysis of a 1x2 Demultiplexer using Cadence Virtuoso**

**Introduction:**A 1x2 Demultiplexer is a combinational logic circuit that takes a single input and routes it to one of the two outputs based on the control signal. It acts as a single-input, two-output switch controlled by a select line. The circuit consists of logic gates (such as AND and NOT gates) implemented using CMOS technology.

The select line determines which output receives the input signal:

1. When the select line is **0**, the input is routed to **Output 0**.
2. When the select line is **1**, the input is routed to **Output 1**.

The CMOS implementation of a 1x2 Demux ensures low power consumption and high-speed operation. Transient analysis helps observe the switching behavior of the circuit, including propagation delays and power dissipation due to capacitive effects.

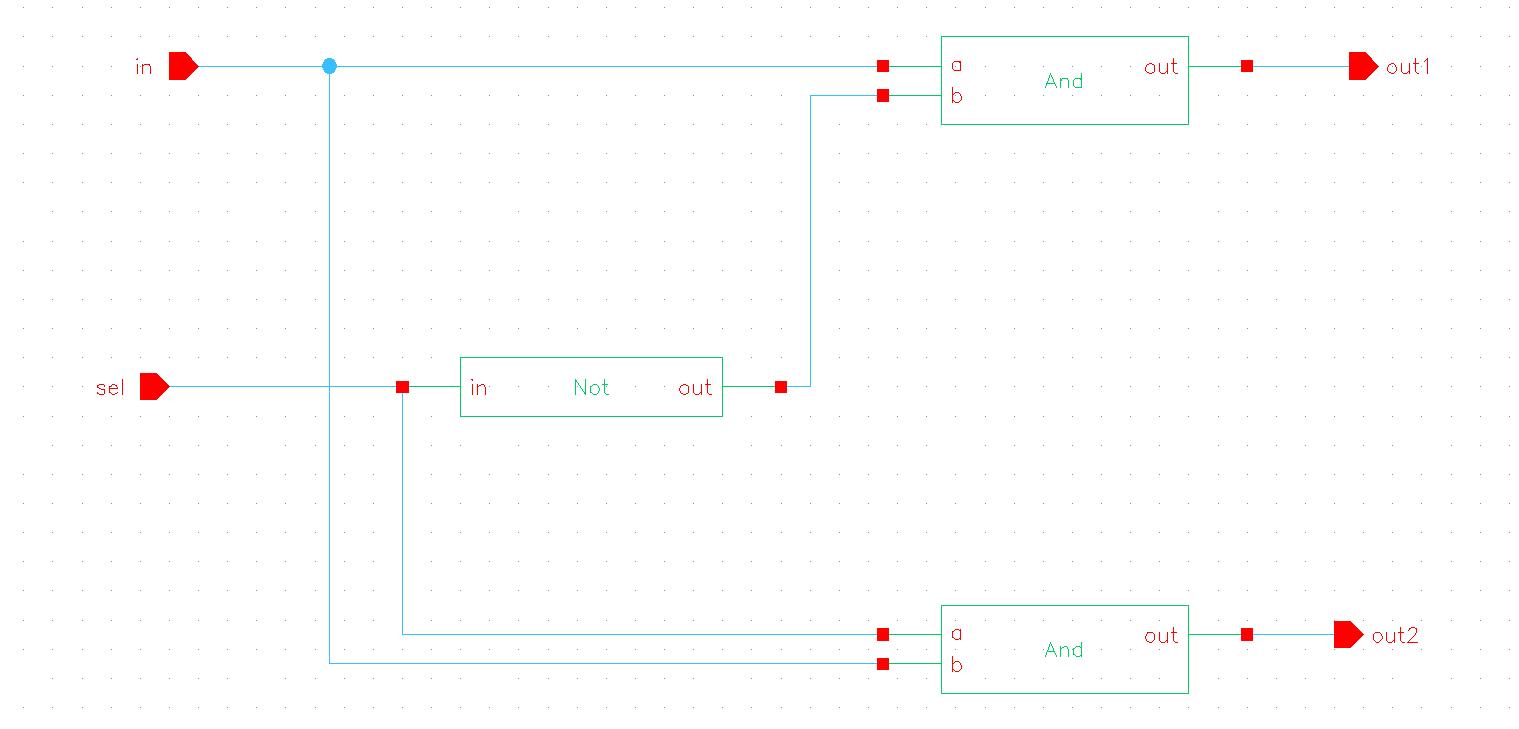
**Circuit Diagram:**

Figure 10.1:Schematic of 1x2 DeMultiplexer

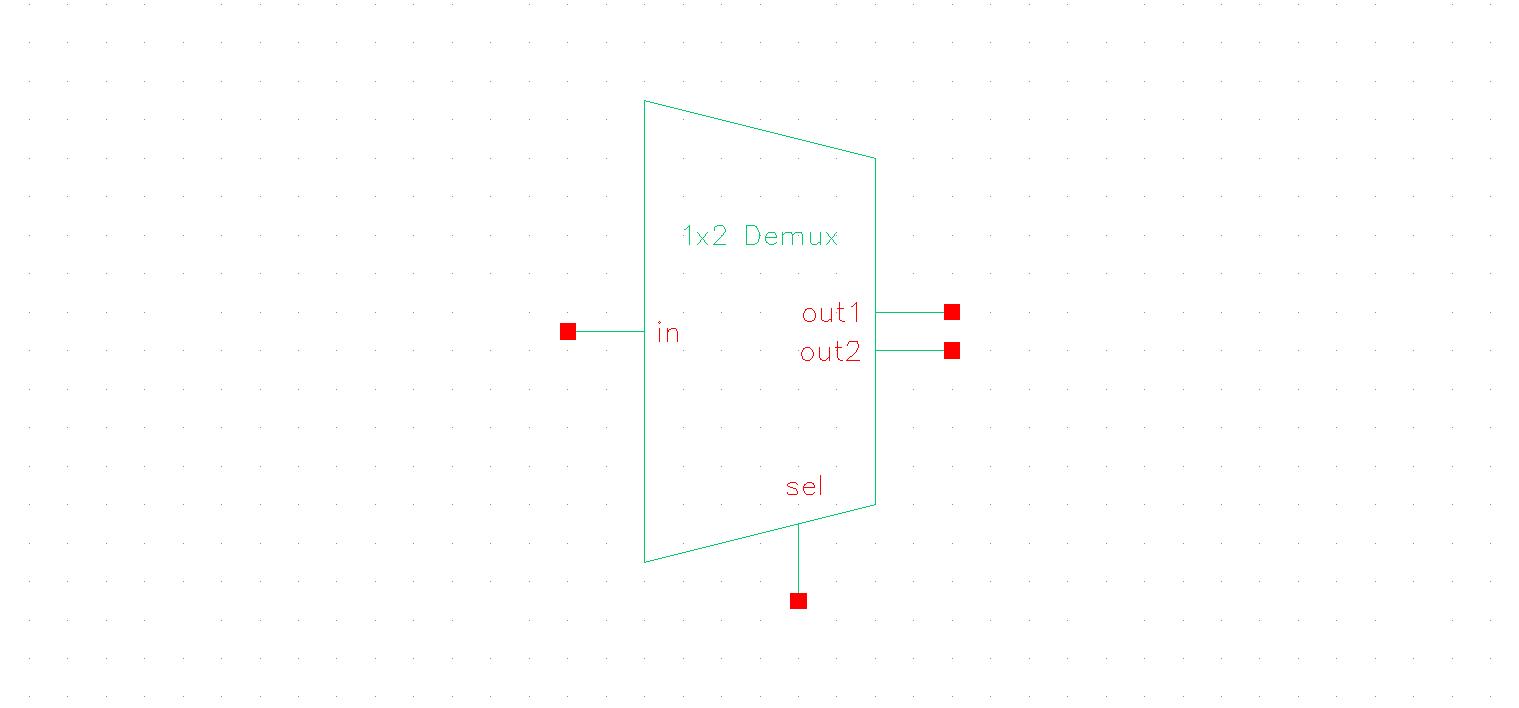


Figure 10.2: Symbol of 1x2 DeMultiplexer

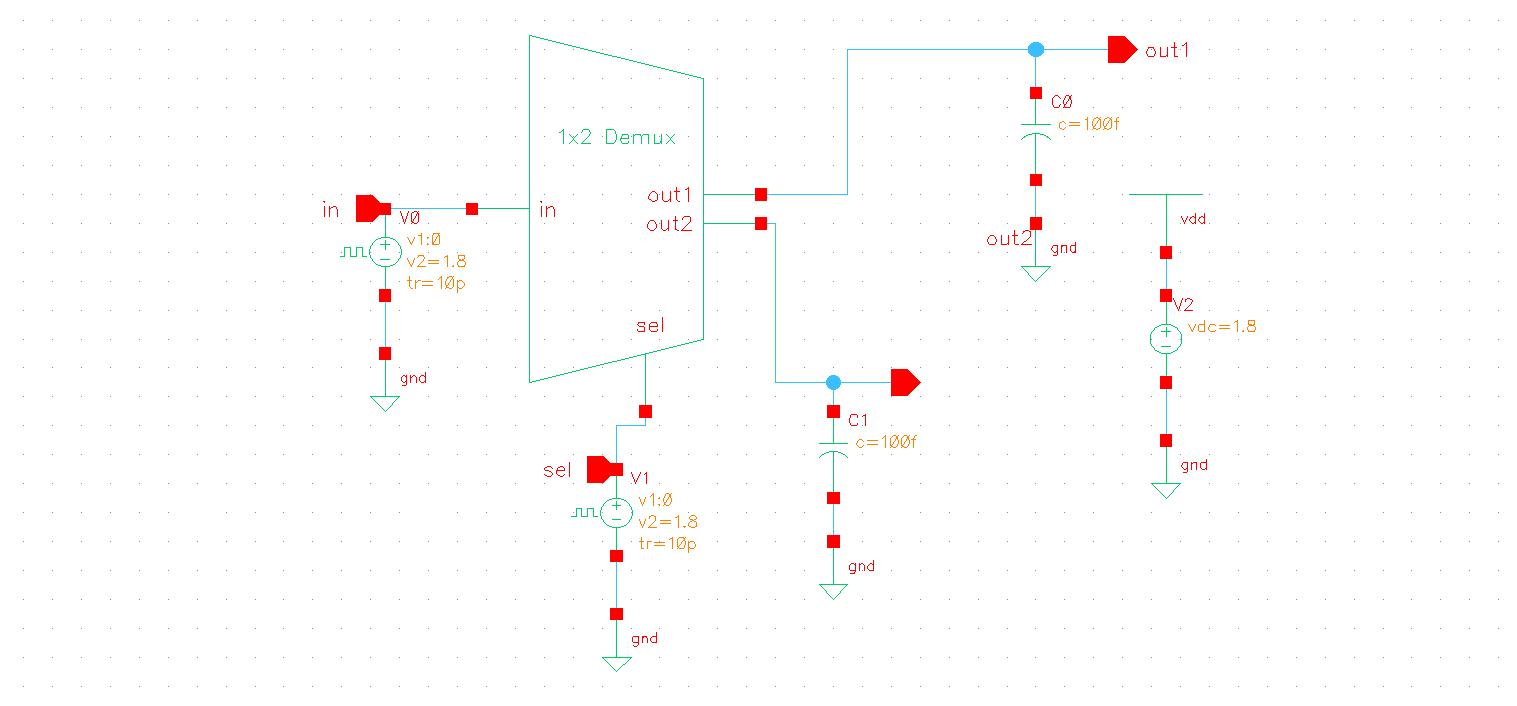


Figure 10.3: Test Schematic of 1x2 DeMultiplexer

**Result:**

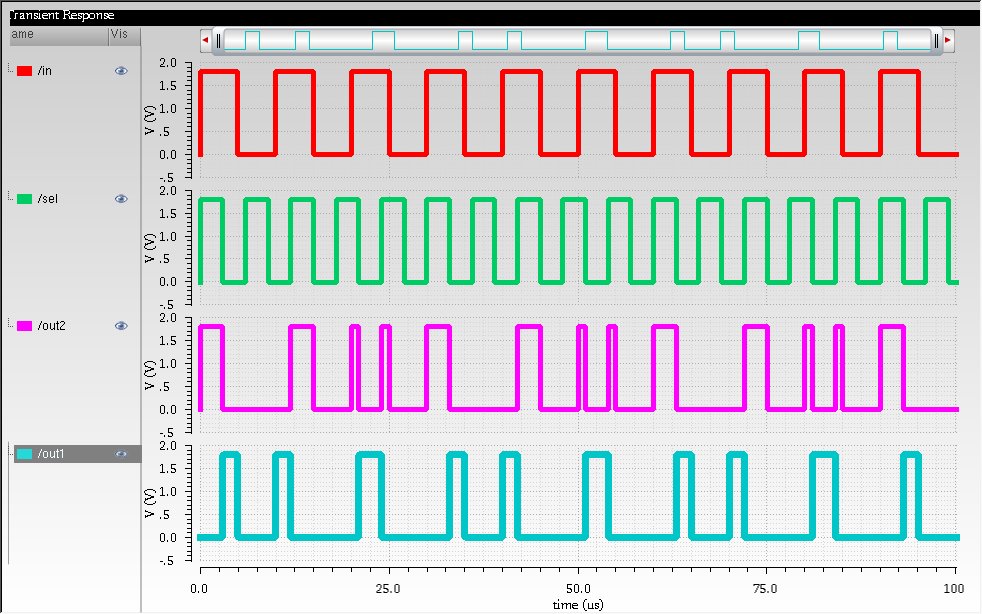


Figure 10.4: Transient Analysis

**Observation:**The CMOS 1×2 Demultiplexer was designed and tested in Cadence Virtuoso, demonstrating correct logic functionality. Transient analysis confirmed that the input signal was successfully routed to the selected output based on the control signal. A small propagation delay was observed, with power dissipation occurring mainly during switching due to capacitive effects. The created Demultiplexer symbol was successfully tested and integrated into circuit design, ensuring its reusability in complex logic circuits.